Title: CMOS Inverter and Integrated Circuits
Utilizing Strained Silicon Surface Channel MOSFETs
Inventor(s): Fitzgerald et al.
Atty Docket No.: ASC-043C2
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV093437255US
Sheet 1 of 13

Strained-Si
channel layer
Relaxed SiGe
SiGe Graded Buffer

Si Substrate

Biaxial Strain

Biaxial Strain

Fig. 1

Inventor(s): Fitzgerald et al. Atty Docket No.: ASC-043C2 Atty/Agent: Steven J. Frank/kb Express Mail Label No. EV093437255US

Sheet 2 of 13

Fig. 2A

Electron Mobility Enhancement vs. Effective Field

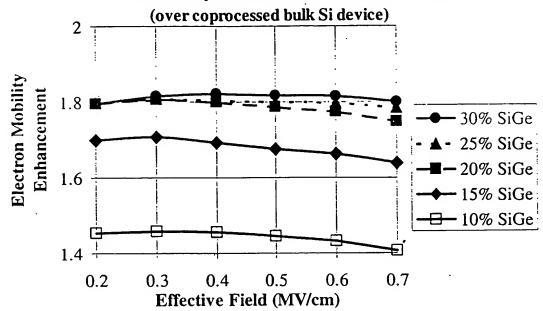
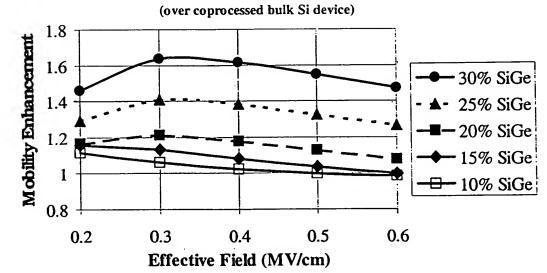


Fig. 2B

Hole Mobility Enhancement vs. Effective Field

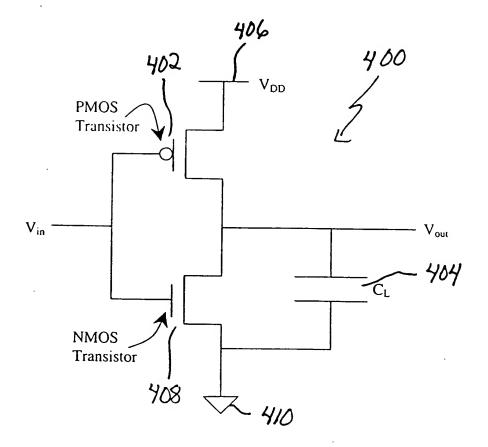


Inventor(s): Fitzgerald et al.
Atty Docket No.: ASC-043C2
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV093437255US
Sheet 3 of 13

Type of Surface	Average Roughness (nm)		
As-grown graded composition relaxed SiGe	7.9		
Planarized SiGe	0.57		
Regrowth SiGe	~0.6		

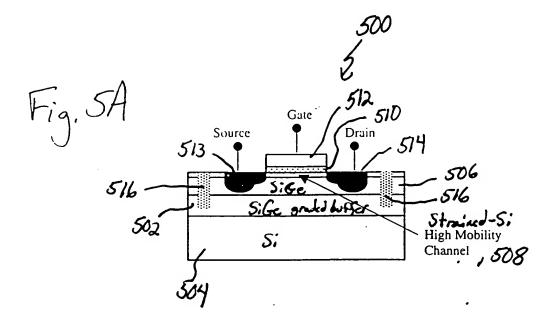
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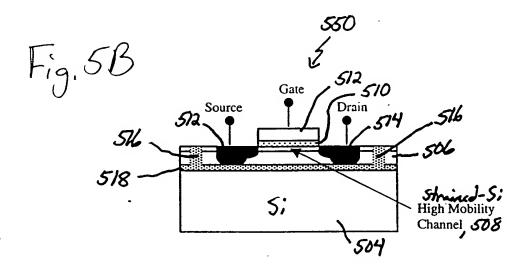
Express Mail Label No. EV093437255US Sheet 4 of 13



Inventor(s): Fitzgerald et al. Atty Docket No.: ASC-043C2 Atty/Agent: Steven J. Frank/kb Express Mail Label No. EV093437255US

Sheet 5 of 13





Title: CMOS Inverter and Integrated Circuits
Utilizing Strained Silicon Surface Channel MOSFETs
Inventor(s): Fitzgerald et al.
Atty Docket No.: ASC-043C2
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV093437255US
Sheet 6 of 13

Sheet 6 of 13

	n enhancement	p enhancement				
Si _{0.8} Ge _{0.2}	1.75	ı				
Si _{0.7} Ge _{0.3}	1.8	1.4				

Fig. 6

Title: CMOS Inverter and Integrated Circuits
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Atty Docket No.: ASC-043C2
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV093437255US
Sheet 7 of 13

	Bulk Silicon	Strained-Si on 20% SiGe: High	Strained-Si on 30% SiGe: High	Strained-Si on 20% SiGe: Low	Strained-Si on 30% SiGe: Low
		Speed Speed Power		Power	
n enhancement	l	1.75	1.3	1.75	1.8
p enhancement	1	1	1.4	1	1.4
W _p (μm)	5.4	5.4	5.4	5.4	5.4
$W_n (\mu m)$	1.8	1.8	1.8	1.8	1.8
$L_n, L_p (\mu m)$	1.2	1.2	1.2	1.2	1.2
C _L (fF)	32	32	32	32	32
$V_{DD}(V)$	5	4.7	4.4	4.3	3.8
NM _H (V)	2.053	2.218	1.949	2.037	1.682
NM _L (V)	2.067	1.654	1.721	1.542	1.504
t _{pHL} (psec)	211.3	133.7	141.6	152.2	180.1
t _{pLH} (psec)	195.8	220.0	173.3	254.8	226.9
t _p (psec)	203.5	176.9	157.4	203.5	203.5
Power (mW)	3.93	3.93	3.93	2.87	2.21
% Speed	-	15.1%	29.3%	•	•
Increase					
% Power	•	•	-	27.0%	43.7%
Reduction					

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Atty Docket No.: ASC-043C2
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV093437255US
Sheet 8 of 13

Sheet	8	of	1	•

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Strained-Si on 30% SiGe:	Low Power	Symmetrical	Inverter	1.8	1.4	6.94	1.8	1.2	. 32	3.5	1.4796	1.4876	204.1	202.9	203.5	1.89	•		52.0%	
Strained-Si on 20% SiGe:	Low Power	Symmetrical	Inverter	1.75	1	9.45	1.8	1.2	32	3.5	1.5018	1.5101	204.4	202.6	203.5	1.95	•		50.4%	
Strained-Si on 30% SiGe:	High Speed	Symmetrical	Inverter	1.8	1.4	6.94	1.8	1.2	32	4.2	1.770	1.781	149.5	143.3	146.4	3.93	39.0%		1	
Strained-Si on 20% SiGe:	High Speed	Symmetrical	Inverter	1.75	1	9.45	1.8	1.2	32	4.3	1.782	1.794	152.0	145.4	148.7	3.93	36.9%		1	
Strained-Si on 30% SiGe:	Constant V _{DD}			1.8	1.4	5.4	1.8	1.2	32	5	2.198	1.923	117.4	139.9	128.6	6.22	58.3%		•	
Strained-Si on 20% SiGe:	Constant V _{DD}		•	1.75		5.4	1.8	1.2	32	5	2.376	1.751	120.7	195.8	158.3	5.06	28.6%		•	
Bulk Silicon				_	1	5.4	1.8	1.2	32	5	2.053	2.067	211.3	195.8	203.5	3.93	•		•	
				n enhancement	p enhancement	W _o (µm)	W _n (μm)	L _n , L _o (μm)	C _L (FF)	· V _{DD} (V)	NM _H (V)	NML (V)	t _{pHL} (psec)	t _{oLH} (psec)	t _p (psec)	Power (mW)	% Speed	Increase	% Power	Reduction

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Atty Docket No.: ASC-043C2
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV093437255US
Sheet 9 of 13

Sheet 9 of 13

	Bulk Silicon	Strained-Si on 20% SiGe: High	Strained-Si on 30% SiGe: High	Strained-Si on 20% SiGe: Low	Strained-Si on 30% SiGe: Low					
		Speed	Speed	····•						
n enhancement	1	1.75	1.8	1.75	1.8					
p enhancement	11	1	1.4	1	1.4					
W_p (μ m)	3.11	4.12	3.53	4.12	3.53					
W_n (μ m)	1.8	1.8	1.8	1.8	1.8					
$L_n, L_p (\mu m)$	1.2	1.2	1.2	1.2	1.2					
C _L (fF)	22.5	26.7	24.2	26.7	24.2					
$V_{DD}(V)$	5	4.5	4.3	4.4	3.8					
$NM_{H}(V)$	2.370	2.275	2.123	2.220	1.872					
$NM_{L}(V)$	1.756	1.485	1.511	1.458	1.371					
t _{pHL} (psec)	148.4	117.3	109.3	12 1 .5	132.4					
t _{pLH} (psec)	238.5	254.8	204.9	265.3	254.4					
t _p (psec)	193.4	186.0	157.1	193.4	193.4					
Power (mW)	2.90	2.90	2.90	2.66	1.83					
% Speed	•	4.0%	23.1%	-	-					
Increase		,								
% Power	-	-	-	8.4%	37.1%					
Reduction		30								

Inventor(s): Fitzgerald et al. Atty Docket No.: ASC-043C2 Atty/Agent: Steven J. Frank/kb Express Mail Label No. EV093437255US Sheet 10 of 13

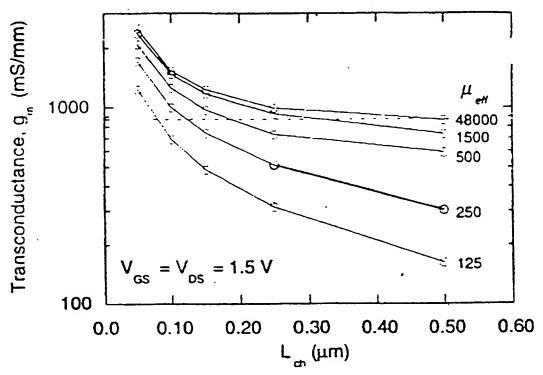
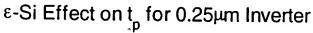


Fig. 10

Inventor(s): Fitzgerald et al.
Atty Docket No.: ASC-043C2
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV093437255US

Sheet 11 of 13



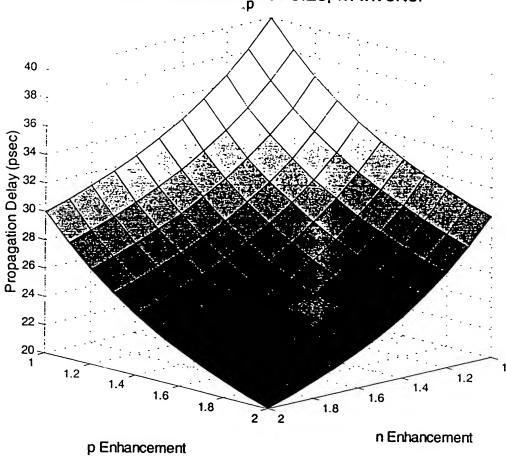
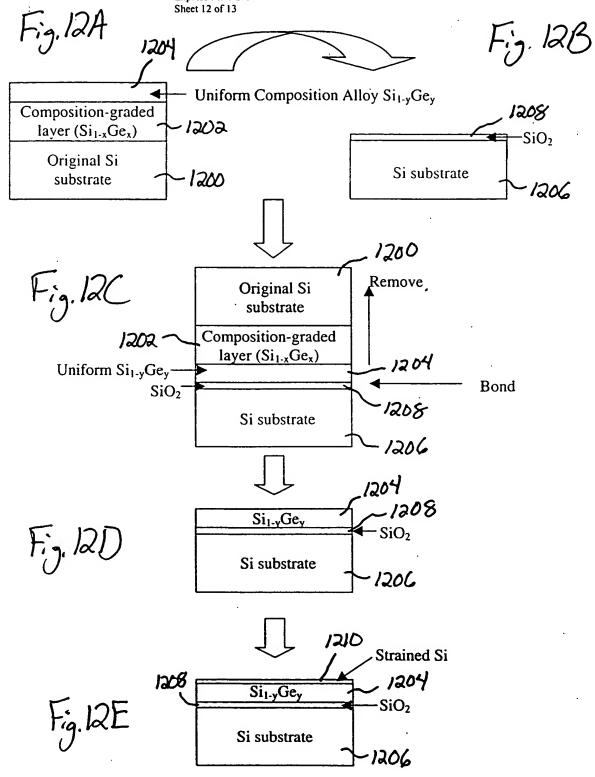


Fig. 11

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